IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Stephen R. Van Doren et al.	§	Confirmation No.:	1168
Serial No.:	10/761,048	§	Group Art Unit:	2446
Filed:	January 20, 2004	§	Examiner:	Farhad Ali
For:	System And Method To Facilitate Ordering Point Migration	§	Docket No.:	200313612-1

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: March 19, 2010

Sir:

Appellants hereby submit this Appeal Brief in connection with the above-identified application. A Notice of Appeal was electronically filed on January 21, 2010.

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I. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P. (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas. HPDC is a wholly owned affiliate of Hewlett-Packard Company (HPC). The Assignment from the inventors to HPDC was recorded on January 20, 2004, at Reel/Frame 014922/0292.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-33.
Claim cancellations:	5, 27, and 29-30.
Added claims:	None.
Presently pending claims:	1-4, 6-26, 28, and 31-33.
Presently appealed claims:	1-4, 6-26, 28, and 31-33.

IV. STATUS OF THE AMENDMENTS

No claims were amended after the final Office action dated December 9, 2009.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

This section provides a concise explanation of the subject matter defined in each of the independent claims, referring to the specification by page and line number or to the drawings by reference characters as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified with a corresponding reference to the specification or drawings where applicable. The citation to passages in the specification or drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element. These specific references are not exclusive; there may be additional support for the subject matter elsewhere in the specification and drawings.

Claim 1 is directed to a system (10, 100) that comprises a first node (12) that broadcasts a request for data and a second node (14, 16, 20) that has a first state associated with the data that defines the second node as an ordering point for the data. Figs. 1-3; P. 3, l. 14 – p 7, l. 11. The second node (14, 16, 20) provides a response to the first node (12) that transfers the ordering point to the first node (12) in response to the request for the data. *Id.* The second node (14, 16, 20) transitions from the first state to a transition state associated with migration of the ordering point to the first node (12). *Id.*

Claim 15 is directed to a computer system (10, 100) that comprises a source processor (12) that issues a broadcast request for desired data while having a first state associated with the desired data. Figs. 1-3; p. 3, l. 14 – p 7, l. 11. The computer system (10, 100) also comprises an owner processor (14) having an associated cache (24) that includes the desired data in a cache line (116). Figs. 1-3; p. 7, ll. 20-31. The cache line (116) has an associated state that defines a copy of the desired data as an ordering point for the desired data. *Id.* The owner processor (14) responds to the broadcast request with an ownership data response that includes the desired data. *Id.* The source processor (12) transitions from the first state to a second state associated with the desired data based on the ownership data response. *Id.* The second state defines the source processor (12) as the ordering point for the desired data. *Id.*

Claim 24 is directed to a system (10, 100) that comprises means (12, 102, 120) for broadcasting a request for data from a first processor node (12, 102) that has a cache state associated with the requested data. Figs. 1-3; p. 3, l. 14 – p. 7, l. 11. The system (10, 100) also comprises means (14, 102, 120; Figs. 1-3; p. 3, l. 14 – p. 7, l. 11) for providing an ownership data response from a second processor node (14, 102) having a cache state that defines the second processor (14, 102) as a cache ordering point for the requested data. Figs. 1-3; p. 3, l. 14 – p. 7, l. 11. The system (10, 100) further comprises means (18, 108; Figs. 1-3; p. 3, l. 14 – p. 7, l. 11) for transferring the cache ordering point from the second processor node (14, 102) to the first processor node (12, 102) associated with the first processor node (12, 102) receiving the ownership data response from the second processor node (14, 102). Figs. 1-3; p. 3, l. 14 – p. 7, l. 11. The system (10, 100) still further comprises means (16, 20, 102; Figs. 1-3; p. 3, l. 14 – p. 7, l. 11) for reissuing a request in the system (10, 100) using a forward progress protocol in response to detecting a conflict while employing a source broadcast protocol in each of the means (12, 102, 120) for broadcasting, the means (14, 102, 120) for providing and the means (18, 108) for transferring. Figs. 1-3; p. 9, ll. 9-31; p. 10, ll. 3-7.

Claim 28 is directed to a method that comprises broadcasting from a source node (12, 102) a request for requested data. Figs. 1-3; p. 3, l. 14 – p 7, l. 11. The method also comprises providing an ownership data response from an owner node (14, 102) in response to the request from the source node (12, 102). *Id.* The method further comprises transitioning a state at the source node (12, 102) associated with the requested data from a first state to a second state in response to receiving the ownership data response, where the second state defines the source node (12, 102) as a new cache ordering point. Figs. 1-3; p. 7, ll. 20-31. The method still further comprises providing a migration acknowledgment signal from the source node (12, 102) to acknowledge receipt of the ownership data response at the source node (12, 102). Figs. 1-3; p. 8, ll. 25-28. The method still further comprises entering a transition state at the owner node (14, 102) in response to providing the ownership data response. Figs. 1-3;

p. 3, l. 14 – p 7, l. 11. The method also comprises releasing the owner node (14, 102) from the transition state in response to the migration acknowledgment signal. Figs. 1-3; p. 9, ll. 1-2.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4, 6-26, 28 and 31-33 are obvious over Rowlands (U.S. Pat. No. 6,993,631) in view of Cypher et al. (U.S. Pat. Pub. No. 2004/0002992).

VII. ARGUMENT: THE EXAMINER ERRED IN REJECTING CLAIMS 1-4, 6-26, 28, AND 31-33 AS ALLEGEDLY OBVIOUS IN VIEW OF ROWLANDS AND CYPHER AT LEAST BECAUSE THOSE REFERENCES FAIL TO TEACH ALL CLAIM LIMITATIONS

A. Summary of Rowlands

Rowlands is directed to the transfer of a coherency block between two nodes. Abstract. A first node requests the coherency block from a second node. Abstract. The second node transfers the coherency block to the first node in response to the request. Abstract. The transfer occurs when a coherency agent resident on the first node performs a transaction to the coherency block resident on the second node. Abstract. A state of the coherency block at the time that block is provided to the first node is recorded in a cache on the first node. Abstract; col. 1, l. 50 – col. 2, l. 20.

B. Claims 1-3, 6, 8-15, 17-18, 20-23

Claim 1 is representative of this grouping of claims. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 U.S.C. § 282 shall apply to each of these claims individually.

Independent claim 1 requires "a second node having a first state associated with the data that defines the second node as an ordering point for the data . . . ." The Examiner rejected this claim in view of Rowlands and Cypher. In particular, the Examiner argues that this limitation is taught in Rowlands' Abstract.

The Examiner errs in making this argument. The portion of the Abstract that the Examiner cites refers to "a state in which the coherency block is provided to the first node," but the portion fails to explain to what that "state" pertains. The Examiner assumes that that "state" pertains to the node from which the ordering point is obtained, as claimed. However, such an assumption is unwarranted and invalid. Rowlands' Summary of the Invention section describes various embodiments, including that which is included in the Abstract, and that Summary section repeatedly and exclusively describes the "state" to be associated with the

coherency block – not a node from which the ordering point is obtained, as claimed. Col. 1, l. 50 – col. 2, l. 20.

The Examiner contends that this limitation is also taught at col. 21, ll. 27-43. Specifically, the Examiner argues that "the second node in the embodiment [of col. 21, ll. 27-43] being the home node is analogous to applicants' second node having a first state associated with the data that defines the second node as an ordering point for the data." Final Office Action, p. 23. The Examiner errs because his citation merely states that "the requesting agent 210 in the node 10A initiates a RdRxc transaction to a cache block for which the node 10B is the home node." Thus, all that is taught is that the node 10B is called a "home node." The Examiner does not cite any teaching that Rowlands' "home" necessarily defines the second node as an ordering point for the data, as claimed.

Based on the foregoing, Appellants respectfully submit that the rejections of the claims in this grouping be reversed and the claims set for issue.

C. Claims 4, 16

Claim 4 is representative of this grouping of claims. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 U.S.C. § 282 shall apply to each of these claims individually.

As established above, the Examiner erred in rejecting claim 1. Claim 4 depends on claim 1. Thus, the Examiner erred in rejecting claim 4.

The Examiner erred in rejecting claim 4 for an additional reason. In particular, claim 4 requires, "wherein the first node comprises a processor having an associated cache that comprises plurality of cache lines, one of the cache lines having an address associated with the data, the second state identifying the one of the cache lines as the ordering point for the data in the system." The Examiner cites col. 2, ll. 4-11 of Rowlands as teaching this limitation. Final Office Action, p. 24.

The Examiner errs, however, because this portion of Rowlands fails to teach the quoted limitation. This portion of Rowlands does appear to teach a

state that is associated with the node that receives the coherency block. Rowlands teaches that this state 1) is retained in the cache; 2) pertains to the coherency block;[1] 3) is recorded by the node sending the coherency block; and 4) is the state in the node that receives the coherency block. Nowhere does Rowlands teach, however, that the state identifies a particular cache line in the cache as the ordering point for the data in the system, as claimed. In fact, Rowlands does not appear to teach that the state identifies any particular cache line for any reason at all. Cypher fails to satisfy Rowlands' deficiencies. Thus, the Examiner erred in rejecting claim 4 for this additional reason.

Based on the foregoing, Appellants respectfully submit that the rejections of the claims in this grouping be reversed and the grouping set for issue.

D. Claims 7, 19, 24-26

Claim 7 is representative of this grouping of claims. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 U.S.C. § 282 shall apply to each of these claims individually.

The Examiner erred in rejecting claim 1, as explained above. Claim 7 depends on claim 1. Thus, the Examiner erred in rejecting claim 7.

The Examiner erred in rejecting claim 7 for an additional reason. Claim 7 requires:

> a multi-processor system implementing a source broadcast protocol, the system further comprising a third node that issues a broadcast request that is received at the second node while in the transition state, the third node reissuing the broadcast request as a request employing an associated forward progress protocol implemented in the system in response to receiving a conflict response from the second node.

[1] The fact that the state pertains to the coherency block corroborates Appellants' argument with respect to claim 1.

The Examiner alleges that the combination of Rowlands and Cypher is configured to selectively transmit coherence requests corresponding to read or write memory operations using a broadcast mode. The Examiner additionally points out that col. 22, ll. 16-33 of Rowlands teaches that an address transfer may be retried or cancelled. While the Examiner's combination does appear to teach some sort of reissuance feature, the combination does not teach Appellants find no teaching in Rowlands concerning "source broadcast protocol," "broadcast[ing]" a request from a third node that is received by a second node at a particular point in time when the second node is in a transition state, reissuance of the request by the third node using a forward progress protocol in response to receiving a conflict response from the second node, etc. Claim 7 is more specific and detailed than a simple teaching of a request reissuance, as taught by Rowlands. Cypher fails to satisfy Rowlands' deficiencies. Thus, the Examiner erred in rejecting claim 7 for this additional reason.

Based on the foregoing, Appellants kindly ask the Board to reverse the rejections against this grouping of claims and to set the claims for issue.

E. Claims 28, 31-33

Claim 28 is representative of this grouping of claims. The grouping should not be construed to mean the patentability of any of the claims may be determined in later actions (*e.g.*, actions before a court) based on the groupings. Rather, the presumption of 35 U.S.C. § 282 shall apply to each of these claims individually.

Claim 28 requires "providing a migration acknowledgment signal from the source node to acknowledge receipt of the ownership data response at the source node." The Examiner asserts that Rowlands, col. 10, l. 65 – col. 11, l. 2 and col. 9, ll. 63-67, teaches this limitation. Respectfully, the Examiner is mistaken. This portion of Rowlands merely teaches acknowledgement of receipt of a "kill command" – not acknowledgement of receipt of the "ownership data response," as claimed. Cypher does not appear to satisfy Rowlands' deficiency. Claims 28 and 31-33 are patentable for at least this additional reason.

The Examiner erred in rejecting claim 28 for yet additional reasons. Claim 28 requires "entering a transition state at the owner node in response to providing the ownership data response" and "releasing the owner node from the transition state in response to the migration acknowledgment signal." The Examiner asserts that Rowlands teaches such limitations at col. 4, ll. 24-37.

Respectfully, the Examiner is mistaken. Rowlands simply does not teach such entry and release of a transition state. Instead, col. 4, ll. 24-37 merely teach about the remote line directory 34. Rowlands teaches that this directory 34 is used to "track the state of the local cache blocks in the remote nodes." Rowlands also teaches that this directory is "updated each time a cache block is transmitted to a remote node, the remote node returns the cache block to the home node, or the cache block is invalidated via probes." However, neither here nor elsewhere does Rowlands teach entry and release of a transition state, as claimed. Further, the Examiner's Arguments section of the Final Office Action fails to address these arguments altogether. Moreover, Cypher fails to satisfy Rowlands' deficiencies. For at least this additional reason, the Examiner erred in rejecting claim 28.

Based on the foregoing, Appellants kindly ask the Board to reverse the rejections against this grouping of claims and to set the claims for issue.

F. Conclusion

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees

required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. A system comprising:

a first node that broadcasts a request for data; and

a second node having a first state associated with the data that defines the second node as an ordering point for the data, the second node providing a response to the first node that transfers the ordering point to the first node in response to the request for the data;

wherein the second node transitions from the first state to a transition state associated with migration of the ordering point to the first node.

2. The system of claim 1, wherein the first node transitions to a second state associated with the data in response to receiving the response from the second node, the second state defining the first node as the ordering point for the data.

3. The system of claim 2, wherein the second state corresponds to a state of a cache line that contains the data, the second state enabling the first node to provide an ownership data response that includes a copy of the data to requests for the data.

4. The system of claim 2, wherein the first node comprises a processor having an associated cache that comprises a plurality of cache lines, one of the cache lines having an address associated with the data, the second state

identifying the one of the cache lines as the ordering point for the data in the system.

6. The system of claim 1, wherein the second node comprises a processor having an associated cache that comprises a plurality of cache lines, one of the cache lines of the second node that contains the data transitioning from the first state to the transition state associated with migration of the ordering point to the first node.

7. The system of claim 1, further comprising a multi-processor system implementing a source broadcast protocol, the system further comprising a third node that issues a broadcast request that is received at the second node while in the transition state, the third node reissuing the broadcast request as a request employing an associated forward progress protocol implemented in the system in response to receiving a conflict response from the second node.

8. The system of claim 7, wherein the forward progress protocol comprises a directory-based protocol.

9. The system of claim 1, wherein the first node provides an acknowledgment signal to the second node after receiving responses from other nodes in the system.

10. The system of claim 9, wherein the second node provides a signal to the first node indicating receipt of the acknowledgement signal.

11. The system of claim 1, wherein the request for the data comprises a request for the data requiring write permission.

12. The system of claim 11, wherein the request for the data further comprises one of a source broadcast read request or a source broadcast write request for the data, and the response from the second node comprises a corresponding ownership data response.

13. The system of claim 1, wherein each of the first and second nodes comprises a processor having an associated cache that comprises a plurality of cache lines, each cache line having a respective address that identifies associated data and state information that identifies a state of the associated data for the respective cache line, each of the processors being capable of communicating with each other via an interconnect.

14. The system of claim 13, wherein each processor further comprises a cache controller that controls the state of the data stored in the plurality of cache lines thereof, at least the cache controller of the first node further comprises a state engine capable of modifying the state information for the cache line

associated with the data to a state that defines the cache line associated with the data as the ordering point based on the response provided by the second node.

15. A computer system, comprising:

a source processor that issues a broadcast request for desired data while having a first state associated with the desired data; and

an owner processor having an associated cache that includes the desired data in a cache line, the cache line having an associated state that defines a copy of the desired data as an ordering point for the desired data, the owner processor responding to the broadcast request with an ownership data response that includes the desired data, the source processor transitioning from the first state to a second state associated with the desired data based on the ownership data response, the second state defining the source processor as the ordering point for the desired data.

16. The system of claim 15, wherein the source processor further comprises a cache line that contains the desired data received from the owner processor, the cache line of the source processor that contains the desired data having an associated state that transitions to a second state in response to receiving the ownership data response from the owner processor, the second state defining the cache line of the source processor that contains the desired data as the ordering point for the data.

17. The system of claim 16, wherein the second state enables the source processor to respond to requests for the desired data by providing an ownership data response that includes a copy of the desired data.

18. The system of claim 17, wherein the state associated with the cache line of the owner processor transitions from a first state to a transition state in connection with providing the ownership data response to the source processor.

19. The system of claim 18, wherein the system employs a source broadcast protocol for controlling the broadcast request issued by the source processor and the response provided by the owner processor, the system further comprising a third processor that issues a broadcast request using the source broadcast protocol that is received at the owner processor while in the transition state, the third processor reissuing the request employing an associated forward progress protocol implemented in the system in response to receiving a conflict response from the owner processor.

20. The system of claim 19, wherein the forward progress protocol comprises a directory-based protocol.

21. The system of claim 15, wherein the source processor provides an acknowledgment signal to the owner processor after receiving a complete set of

responses from the system, the acknowledgement signal enabling the owner processor to transition from a transition state to an invalid state.

22. The system of claim 21, wherein the owner processor provides a signal to the source processor indicating receipt of the acknowledgement signal.

23. The system of claim 15, wherein the owner processor provides a blocking signal to prevent a home node from responding with a copy of the desired data in response to receiving the broadcast request from the source processor.

24. A system, comprising:

means for broadcasting a request for data from a first processor node having a cache state associated with the requested data;

means for providing an ownership data response from a second processor node having a cache state that defines the second processor as a cache ordering point for the requested data;

means for transferring the cache ordering point from the second processor node to the first processor node associated with the first processor node receiving the ownership data response from the second processor node; and

means for reissuing a request in the system using a forward progress protocol in response to detecting a conflict while employing a

source broadcast protocol in each of the means for broadcasting, the means for providing and the means for transferring.

25. The system of claim 24, further comprising means for providing a migration acknowledgment signal to acknowledge receipt of the ownership data response at the first processor node and for transitioning to a cache state at the first processor node that defines the first processor node as the cache ordering point.

26. The system of claim 25, further comprising means for acknowledging receipt of the migration acknowledgment signal by the second processor node.

28. A method comprising:

broadcasting from a source node a request for requested data;

providing an ownership data response from an owner node in response to the request from the source node;

transitioning a state at the source node associated with the requested data from a first state to a second state in response to receiving the ownership data response, the second state defining the source node as a new cache ordering point;

providing a migration acknowledgment signal from the source node to acknowledge receipt of the ownership data response at the source node;

entering a transition state at the owner node in response to providing the ownership data response; and

releasing the owner node from the transition state in response to the migration acknowledgment signal.

31. The method of claim 28, wherein the source node and the owner node employ a source broadcast protocol, the method further comprising:

issuing a broadcast request for the requested data from a third node using the source broadcast protocol; and

reissuing the broadcast request from the third node as a request using a forward progress protocol in response to the owner node being in the transition state when the owner node receives the broadcast request issued by the third node.

32. The method of claim 28, further comprising providing an acknowledgment signal to the source node to acknowledge receipt of the migration acknowledgment signal at the owner node.

33. The method of claim 28, wherein the source node comprises a processor node that includes a cache having a plurality of cache lines, one of the cache lines of the processor node containing the requested data based on the ownership data response and having a state associated therewith, the state

associated with the one of the cache lines defining the source node as the new cache ordering point.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.